

**REMARKS**

Applicant has carefully reviewed and considered the Office Action mailed on September 22, 2003, and the references cited therewith.

Claims 1, 2, and 29 are amended, and no claims are cancelled or added; as a result, claims 1-29 remain pending in this application.

**Request for Information**

Applicant and the assignee of this application are required under 37 CFR 1.105 to provide certain information that the examiner has determined is reasonably necessary to the examination of this application.

Figures 2 and 3, referenced in the Office Action, were not taken from published material that may be relevant to prosecution of this matter, but are instead drawings taken from the client's invention disclosure. Because such communication is not public in nature and is subject to attorney-client privilege, it is not attached hereto. Applicant regrets that he is not aware of any similar publicly available references that may serve as a substitute reference for examination purposes.

**§103 Rejection of the Claims**

Claims 1-29 were rejected under 35 USC § 103(a) as being unpatentable over Drako et al. (U.S. 5,371,877) in view of Rust et al., (U.S. 5,699,530).

Drako discusses implementing a dual port FIFO memory by using two banks of single-port RAM, and an apparatus for interleaving reads and writes between banks such that successive writes will be to different memory banks, and such that the memory bank not being written may be read.

Rust describes a circular RAM-based FIFO buffer using interleaved storage and cross pointers. A first RAM bank stores even data, and a second RAM bank stores odd data. A read pointer and a write pointer use shift registers to select the written or read element.

The present invention, in contrast, comprises a system and method for employing a dual-ported FIFO memory to manage memory timing issues between an SDRAM data bank and a memory controller. Independent claim 1 and dependent claim 2 of the present invention have

been amended to more clearly distinguish the structure and function of the present invention from the cited references, which are not designed to achieve such a function. The original claims further recited banks of memory operable to buffer memory data, which distinguishes them from the cited references. Claims 10, 20, and 29 already incorporate such limitations, but claim 29 has been amended to clarify the context and application of various recited elements.

DEC 29 2003



**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Serial Number: 09/619771

Filing Date: July 20, 2000

Title: DUAL-BANK FIFO FOR SYNCHRONIZATION OF READ DATA IN DDR SDRAM

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Dkt: 499.078US1

Conclusion

Applicant respectfully submits that the amended claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9581 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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Date

Dec 22 03

By

  
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of December, 2003.

Name

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Signature

